STABILIZATION METHOD FOR DRAIN VOLTAGE IN NON-VOLATILE MULTI-LEVEL MEMORY CELLS AND RELATED MEMORY DEVICE

Field of the Invention

[0001] The present invention relates to electronic circuits, and, more particularly, to memory devices and related methods.

Background of the Invention

[0002] During programming of a Flash memory cell, it is important to properly set the voltage applied to the various terminals thereof (i.e., gate, source, drain, and body terminals). In the multi-level flash memory field where the cell is programmed at different threshold voltage values, node stability becomes an even more critical problem.

[0003] The simple case of programming a multi-level cell with two bits per cell will now be considered, i.e., a two-level cell with four possible combinations of storable logic values. Turning now to FIG. 1, the distributions of four different programming states of such a cell (i.e., the distributions of its possible threshold voltage values), are shown. The programming step of a Flash cell is typically preceded by an erasing step. Consequently, in the beginning the cell is brought to the logic state 11, the state with the lowest threshold.

[0004] The programming algorithm may be split into n

substantially identical steps. In the first part of each of these steps, the Flash memory cell is biased to keep the drain node at a fixed voltage value (typically +4V), the source node to ground, and the body at a fixed negative value (typically -1.2V). The gate node is initially set at a voltage of 1.5V, and is then increased in subsequent steps, for example, by 300mV at each further step. This leads to an increase in the cell threshold voltage in steps, as illustrated in FIG. 1.

[0005] In the second part of each programming step, the state of the cell is tested through a reading operation (verify). If the cell does not reach the desired distribution, the operation is repeated by increasing the gate voltage. If, on the other hand, the cell threshold voltage reaches the desired distribution, the programming thereof ends.

[0006] The programming step typically does not involve only one cell, rather a certain number of cells are programmed in parallel. When one or more cells reach the desired threshold value (i.e., it reaches the desired threshold distribution), they are excluded from the following programming step which continues only for the remaining cells that have yet to reach the predetermined state.

[0007] In some fairly recent prior art memory devices, the programming step involves programming about seventy cells in parallel, which results in a variable current load for the drain voltage regulator during the different programming steps. The changes of the threshold voltage and the applied gate voltage cause a different current absorption by the memory

cells. Moreover, when the cells have reached the desired state, they are disconnected through a program load transistor, for example, as shown in the schematic circuit diagram of FIG. 2.

[0008] It will therefore be understood that the cell drain voltage regulator, in the different programming steps, has to provide a constant voltage value, but in different current load conditions. The drain voltage **VPD** (+4V) is derived from the band gap reference voltage **(VGB)** according to the following relation:

$$V_{PD} = V_{BG} \cdot \left(1 + \frac{R_f}{R_g}\right),$$

which expresses the gain of a feedback voltage amplifier in a non-inverting configuration.

[0009] The drain regulator, for layout requirements, may be at a certain distance from the program load transistors **PL**. The interconnection metal line bringing the adjusted voltage **VPD** to these transistors, inserts a parasitic resistance, quantifiable in some tens of ohms. Considering that each memory cell can absorb a drain current of about 60μA, with seventy cells being programmed the total current can reach 4mA. With a parasitic resistance **Rpars** for the metal line equal to 25Ω, as shown in FIG. 3, the voltage drop thereon can reach up to 100 mV. Since the cells which have reached the appropriate distribution are disconnected from the adjusted voltage **VPD**, the cells upon which programming continues may have a drain voltage changed by +100mV in some cases.

[0010] Some typical curves showing the threshold

voltage change in the programming step according to different drain voltage values are schematically represented in FIG. 4. In the illustrated diagram, the abscissa indicates the gate voltage, and the ordinate indicates the threshold voltage. If the drain voltage is constant during all of the programming steps, the cell threshold voltage change follows one of these characteristics. If, on the other hand, the drain voltage changes during programming, the threshold voltage change translates in another characteristic. This results in a higher threshold jump and a widening of the distributions associated with the circuit of FIG. 1 with a corresponding decrease in the reading noise margin or, in the worst case, in real failures due to an excessive distribution widening.

Summary of the Invention

[0011] The technical problem underlying the present invention is to provide a method for stabilizing the drain voltage and a corresponding non-volatile memory device having respective functional and structural characteristics which improve the Flash cell drain voltage stability. Moreover, this is to be done while avoiding the use of voltage regulators positioned near the cell drains. As noted above, drain voltage is influenced by the change in the current absorption during the different programming steps.

[0012] The premise underlying the present invention is to provide the feedback potential of the voltage regulator corresponding to the program load transistors away from the regulator output. This is done to make the voltage on the load node independent from the

parasitic resistance on the metal line and from the variable current load.

[0013] The present invention relates to a multi-level, non-volatile memory device monolithically integrated on a semiconductor which may include a programming circuit associated with a matrix of non-volatile memory cells. Each memory cell may be equipped with at lest one floating gate transistor with corresponding source, drain and gate terminals. Each programming circuit may incorporate a drain voltage regulator having an output connected to the cell drain terminals in a common circuit node, and through a metal line conduction path having a parasitic intrinsic resistance.

[0014] Furthermore, the invention relates to a method for stabilizing the voltage at both ends of a load among a plurality of loads associated with a supply line, the loads being active one at a time. The application of the voltage may be provided through a voltage regulator having an output connected to the loads by the supply line and a plurality of routing resistances, each being associated with a corresponding load.

Brief Description of the Drawings

[0015] The various features and advantages of the present invention will be further understood from the following description of an embodiment thereof given by way of non-limiting example, with reference to the attached drawings, in which:

[0016] FIG. 1 is a diagram illustrating the threshold voltage distribution in a prior art two-level

memory cell with two bits per cell;

[0017] FIGS. 2 and 3 are schematic diagrams of prior art programming circuits of the program-load type;

[0018] FIG. 4 is a voltage/voltage diagram illustrating curves which are typical of a prior art multi-level memory cell;

[0019] FIG. 5 is a schematic diagram generally illustrating a first embodiment of the present invention;

[0020] FIG. 6 is a schematic diagram of a second embodiment of the present invention;

[0021] FIGS. 7A and 7B are schematic diagrams illustrating a circuit according to the prior art and according to the present invention, respectively, for comparison purposes;

[0022] FIGS. 8A-8C are graphs respectively showing the evolution of voltage signals and current in a device according to the invention over time compared to a prior art device; and

[0023] FIGS. 9A-9D are schematic diagrams illustrating an exemplary implementation of the present invention for a plurality of loads distributed along a resistive line.

Detailed Description of the Preferred Embodiments

[0024] Referring now to FIGS. 5 and 6, a circuit portion **1** of an electronic memory device according to the present invention is first described. The circuit portion **1** is structured to locally regulate voltage values on the drain terminals of multi-level non-volatile memory cells **3** during programming thereof. More particularly, the circuit portion **1** refers to a

drain regulator **2** connected to a common load circuit node **A** by a metal line **4**.

[0025] The memory matrix columns, i.e., the drain terminals of the memory cells **3**, are connected to the circuit node **A** via a respective program load transistor **PL**. As used herein, "memory device" means any monolithic electronic system incorporating a matrix of memory cells, organized in rows and columns, as well as circuit portions associated with the cell matrix and responsible for the addressing, decoding, reading, writing and/or erasing of the memory cell contents. Such a device may be, for example, a semiconductor-integrated memory chip of the non-volatile EEPROM Flash type split into sectors that is electrically erasable.

[0026] Each multi-level memory cell comprises a floating gate transistor with source **S**, drain **D** and control gate **G** terminals. Programming circuits are provided among the circuit portions associated with the cell matrix, and each programming circuit is supplied by a specific supply voltage generated inside the integrated memory circuit and regulated by the drain voltage regulator **2**.

[0027] In accordance with the present invention, the node **A** is feedback-connected to an input of the regulator **2**. The parasitic resistance $\mathbf{R_{pars}}$ on the metal line is therefore substantially incorporated in the feedback loop.

[0028] In accordance with a first exemplary embodiment of the invention, the drain voltage regulator **2** is output-connected to the node **A** by the metal line **4**, and has an input feedback-connected to the same node **A**. A first gain resistor **Rf** and a second

resistance R_{parf} representing the parasitic resistance of the feedback metal line **5** are illustratively indicated on the feedback path.

[0029] The series of resistances **RF** and R_{parf} is thus a resistive value which can be assigned to this feedback connection. The regulator **2** input receiving the feedback is the inverting input (-). The other (non-inverting) input is kept at a stable voltage reference, for example, a bandgap voltage **Vbg**. This configuration makes the node **A** voltage independent from the parasitic resistance R_{pars} value, and thus from the variable current load.

[0030] As a result, the feedback node advantageously is no longer at the regulator **2** output as in the prior art, but it is instead near the program load transistors **PL**. The interconnection parasitic resistance R_{pars} is thus incorporated inside the feedback loop. Moreover, since the node **OUT** is no longer fed back to the inverting amplifier input, but instead the node **A** is fed back, this allows a voltage value regulated to **4V** to be kept on the node **A**. More particularly, the voltage is not regulated to **4V** at the voltage regulator **2** output, but at the load node **A**. The node **OUT** is thus regulated by the feedback to obtain **4V** on the node **A**.

[0031] The voltage at the node **OUT** will vary based upon the load current according to the following relation:

$$V_{OUT} = Iload * Rpar + V_{NODA} ;$$

while the voltage on node **A** satisfies the following

formula:

$$VnodoA = V_{BG} \cdot \left(1 + \frac{R_f + R_{parf}}{R_g}\right),$$

where **Rparf** is the parasitic resistance of the feedback metal line **5** (which is typically equal to about a few hundred ohms), and it can be also ignored if **Rf** is high enough. This parasitic resistance **Rparf**, once estimated, does not cause voltage changes at the node **A** since the load current does not flow in this resistance.

[0033] Turning more particular to the example illustrated in FIG. 6, an alternative embodiment of the present invention is now described. In this second embodiment a unitary gain buffer **7**, for example, of the voltage-follower type, is inserted immediately downstream of the drain voltage regulator **2**. This embodiment, while preserving the advantages of the previous solution, has the further advantage of substantially eliminating the effect of the parasitic resistance $\mathbf{R_{parf}}$ of the feedback metal line **5**.

[0034] More specifically, the feedback node **A** is connected once again downstream of the resistance $\mathbf{R_{pars}}$ and not at the regulator **2** output. This keeps the voltage upstream of the program load transistors equal to the voltage **VPD** at inputting buffer **7**, and the gain (unitary) of the latter is not influenced by the resistance $\mathbf{R_{parf}}$.

[0035] FIGS. 7A and 7B are schematic diagrams respectively illustrating a prior art circuit (i.e., similar to the one illustrated in FIG. 2) and a circuit in accordance with the present invention (i.e., similar

to the one illustrated in FIG. 5). Moreover, FIGS. 8A, 8B and 8C illustrate the evolutions of voltage values according to the current load for these circuits for comparison purposes, with the prior art results illustrated with short dashed line (and "◊" symbols), and the results of the present invention illustrated with solid or continuous lines (and "+" symbols).

[0036] The methods and devices according to the present invention are particularly effective in situations requiring a plurality of loads belonging to a same resistive line (and not necessarily memory cells connected to a same metal line), which are to be supplied with constant regulated voltages. Turning to the example illustrated in FIG. 9A, load sources **L0**, **L1**, …, **LN** are spaced from one another (and thus have different routing resistances **Rpars0**, **Rpars1**, …, **RparsN**, associated therewith) and are to be supplied with different voltages VREF.

[0037] In this case line **4** is a supply line which, starting from the output of the regulator **2**, distributes the voltage to the loads across the routing resistances **Rpars0**, **Rpars1**, …, **RparsN** associated with each load. A node **F** near the farthest load **LN** from the regulator is the node to be used for the feedback connection **5** of the regulator **2**.

[0038] For the present example it will be assumed that only load **L1** absorbs current (i.e., the others are off or otherwise absorb no current). On the node **A** connected to load **L1** the desired voltage **VREF** is reached. On the right of the node **A** there is no current absorption, since the current generators to the right thereof are off. Moreover, the inverting input of the

regulator **2** has a high impedance since it is generally formed by the gate terminal of a MOS transistor.

[0039] If the load **L1** is now deactivated, and in the meantime another load is enabled (e.g., load **L4**), the voltage **VREF** reaches the node to which the load **L4** is connected, which is also indicated in FIG. 9C as node **A**. Thus, the voltage supplied to each single load is stable against changes which occur from time to time.

[0040] Accordingly, the method and the devices according to the present invention solve the technical problem noted above and allow the voltages at the drain memory cell terminals to be stabilized during the multi-level Flash memory programming steps. Moreover, the present invention, by keeping the value of these voltages stable during programming, allows gate pulses applied during the programming algorithm to effectively realize a threshold voltage jump which is constant for each pulse with various programming patterns.